REMARKS

I. Introduction

In response to pending Office Action, Applicants have amended the Title of Invention, the specification and the drawings so as to address the pending objection to the title and informalities in the specification and drawings. Applicants have also amended claim 4 so as to further clarify the claimed subject matter. No new matter has been added.

For the reasons set forth below, it is respectfully submitted that all pending claims are patentable over the cited prior art references.

II. The Rejection of The Claims Under 35 U.S.C. § 102(b)

Claims 1-3, 5, 7-10 and 12-15 are rejected under 35 U.S.C. § 102(b) as being anticipated by USP No. 5,506,976 to Jagger. This rejection is respectfully traversed for the following reasons.

In accordance with the present invention, the processor comprises: 1) an execution instruction address outputting means for outputting an execution instruction address that is an address of an area in which an instruction to be executed by the instruction executing means is stored, and 2) detecting means for detecting that the instruction to be executed by the instruction executing means is a last instruction of a process before branching, wherein the execution instruction address outputting means outputs a start address that is an address of an area in the storing means in which a first instruction of a process after branching is stored, when the last instruction is detected by the detecting means.

Turning to the prior art, at a minimum, Jagger fails to disclose or suggest an execution instruction address outputting means for outputting a start address that is an address of an area in

the storing means in which a first instruction of a process after branching is stored, when the last instruction is detected by the detecting means.

Specifically, the Examiner asserts that the program counter 10 of Jagger corresponds to the execution instruction address outputting means of the present invention, and the program counter 10 outputs a start address "&U" of a first instruction "U" of a process, when the last instruction E is detected. However, Jagger only discloses that the program counter 10 stores a program counter value PC that represents the address of the instruction to be fed to the pipeline 2 (see Jagger, col. 6, lines 47-48). The Jagger reference does not expressly disclose or suggest that the address it represents is necessarily the start address. As such, the Jagger reference fails to disclose or suggest that the execution instruction address outputting means outputs a start address, as currently recited by claim 1.

Furthermore, the Examiner asserts that the main memory system 8 corresponds to the claimed storing means (see, page 4, item 10 of Office Action). However, Jagger does not disclose or suggest that the first instruction of a process after branching is stored in the main memory system 8. Rather, main memory system 8 is used merely for transferring instructions into instruction fetch stage 8 (see Jagger, col. 6, lines 43-45). Indeed, Jagger discloses that the target address is stored in the branch cache 4, as shown in Fig. 4, Further, the branch cache 4 does not store this target address if the enable signal is in the OFF state (see, col. 8, lines 1-14). Therefore, at a minimum, Jagger fails to disclose or suggest a start address that is an address of an area in the storing means in which a first instruction of a process after branching is stored, as recited by the rejected claim.

Moreover, the Jagger reference does not disclose or suggest that the detecting means for detecting that the instruction to be executed by the instruction executing means is a last

instruction of a process before branching. Rather, the comparator 14 of Jagger compares the contents of the reach value latch 16 with the program counter value PC in the program counter 10 to determine if their values match. If the comparator 14 determines that the reach value R currently stored within the reach value latch 16 matches the lowermost 8 bits of the program counter value PC stored within the program counter 10, a cache hit occurs and a hit signal is asserted ON which causes the reach value latch 16 to latch in the new reach value "&X" and the target address latch 18 and target instruction latch 20 to output their contents "&U" and U to the program counter 10 and instruction fetch stage 6, respectively (see Jagger, col. 6, lines 1-35). Therefore, the detecting means of Jagger does not detect the last instruction of the process, but detects the lowermost 8 bits of the program counter value and reach value. Thus, at a minimum, it is clear that the detecting means of Jagger does not correspond to the claimed detecting means for detecting that the instruction to be executed by the instruction executing means is a last instruction of a process before branching.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, ***Kalman v. Kimberly-Clark Corp.***, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), for the foregoing reasons, it is clear that Jagger does not anticipate claim 1 or any claim dependent thereon.

III. The Rejection of The Claims Under 35 U.S.C. § 103

Claim 4 is rejected under 35 U.S.C. § 103 as being unpatentable over Jagger in view of USP No. 6,304,962 B1 to Nair and USP No. 5,898,866 to Atkins. This rejection is respectfully traversed for the following reasons.

In accordance with the present invention, the comparator 236 compares the relative address stored in the program counter 134 with the processing length selected by the selector 232, as readily shown in Fig. 7 and step ST24 of the present invention (see, e.g., page 24 of the specification). The foregoing process allows the processing of the program modules to be sequentially performed without instruction cycles for branching so as to reduce the total processing time. In addition, since the processing length having small amount of data is used instead of the end address that is an absolute address, the hardware scale for storage of data, selection and comparison is further reduced.

Turning to the prior art, nowhere in the disclosure of the cited prior art does it disclose or suggest a processing length selecting means for sequentially switching and selecting the processing length stored in the processing length storing means, as currently recited by claim 4. Indeed, the Examiner has not expressly stated what constitutes the corresponding processing length selecting means and how sequentially switching and selecting are accomplished. Thus, at a minimum, the combination of Jagger in view of Nair and Atkins fails to disclose or suggest a processing length selecting means for sequentially switching and selecting the processing length stored in the processing length storing means. As such, for at least these reasons, it is respectfully submitted that claim 4 is patentable over the cited prior art.

IV. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, ***Hartness International Inc. v. Simplimatic Engineering Co.***, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that claims 2-20 are also in condition for allowance.

Furthermore, in accordance with the present invention, the address storage device 100 stores the start and end address of each program module, and the selection of the start and end address is switched when the current execution instruction address is matched with the end address by hardware (i.e. without executing a branching instruction). The foregoing process allows the processing of the program modules to be sequentially performed without instruction cycles for branching, thus reducing the total processing time (see, e.g., page 22 of the specification).

In contrast, nowhere in Jagger's disclosure does it disclose or suggest a start or end address selecting means for sequentially switching and selecting the start or end address stored in the start or end address storing means, as recited by claims 2 and 3 respectively. Indeed, the Examiner has not expressly stated what constitutes the corresponding start and end address selecting means and how sequentially switching and selecting are accomplished. Thus, at a minimum, the Jagger reference fails to disclose or suggest a start or end address selecting means for sequentially switching and selecting the start or end address stored in the start or end address

storing means. As such, for at least these reasons, it is respectfully submitted that claims 2 and 3 are patentable over the cited prior art.

Finally, it is noted that Jagger does not disclose or suggest that the start or end address stored in the start or end address storing means for the supervisory processor is written in the start or end address storing means at a predetermined timing, as currently recited by claims 10 and 15 respectively. Indeed, Jagger does not disclose or suggest any predetermined timing in the branch cache 4. As such, for the foregoing reasons, it is respectfully submitted that claims 10 and 15 are patentably distinct over the cited prior art.

V. Request For Notice Of Allowance

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, an additional petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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